examination.

BACKGROUND

The invention is a stacked MCM package in which both RF and digital MCMs are stacked on top of one another. In the prior art, as represented by applicants' Fig. 5, the digital and RF IC chips, or digital and RF MCMs, were separated laterally on the substrate. This was to avoid interference between the two types of IC devices. It is known that RF IC chips are sensitive to noise that arises from stray fields, for example, those from digital chips. Therefore nowhere in the prior art that is known to applicants, and surely not in the prior art that is cited in this record, are digital and RF IC chips or MCMs stacked one on top of the other. That is the invention claimed in claim 1, for example, and is essentially claimed in every claim pending. The claimed stacked arrangement is made possible, and inter chip interference avoided, by isolating the digital chips from the RF chips in the stack. The I/Os in the RF MCM are isolated from the digital MCM by routing dedicated RF I/O interconnections straight through the digital MCM, without any electrical connections to the digital MCM. The invention is shown clearly in Figs. 6 and 7.

RESTRICTION REQUIREMENT

In the first Office action, election of species was required. Applicants traversed the requirement on the ground that the requirement was improper and that all claims in the application read on all of the figures that were identified as separate species. The requirement has been made final. Applicants continue to object to the requirement as improper, and preserve their position for future deliberations.

To be responsive, applicants elected Fig. 3, even though Fig. 3 is not a distinct species of the invention. As requested in the last Office action, the Examiner is asked to state specifically what in claim 2, for instance, makes that claim not readable on Fig. 3, the elected figure.

DRAWING

Evidently the objection to the drawing, made in the prior Office action, is no longer maintained.

REJECTION

Claims 1 and 21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art in view of Akram et al.

Claim 10-12 and 19-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art in view of Akram et al. and further in view of Vendramin.

ARGUMENT

Rejection under 35 U.S.C. 103(a) – claims 1 and 21

Claims 1 and 21 stand rejected as unpatentable over applicants' Fig. 5 in view of Akram et al. As discussed above, the invention claimed in these claims includes the combination of an RF IC chip and a digital IC chip in a stacked arrangement with the RF IC chip electrically isolated from the digital IC chip. These claims then have these three

features:

1. RF IC chip plus digital IC chip
2. Stacked RF IC chip and digital IC chip arrangement
3. RF IC chip in stack electrically isolated from digital IC chip.

According to the rejection, applicants Fig. 5 shows feature 1. It clearly does not show the combination of features 2. and 3. The Office action states that unequivocally. So evidently, Akram et al. is relied on for teaching features 2. and 3. But Akram et al. never even mentions feature 1., and thus clearly does not show the combination of features 1., 2. and 3., or the combination of Figs. 2. and 3. In fact, since Akram et al. never mention RF IC chips that patent is not even relevant to the issue.

In supporting the obviousness of the rejection, the Office action merely concludes that the claimed combination would be obvious. Akram et al. shows an arrangement with stacked digital IC chips. There is no suggestion whatever to include an RF IC chip in that stack. It would not be obvious to do that because of the problem applicants' invention is designed to overcome, i.e. signal interference. Nor is there any suggestion of how to overcome that problem, i.e. the routing of electrical leads through the digital IC chips in a passive manner, i.e. electrical isolation. So there is no recognition in the Akram et al. patent of the problem overcome by the invention (that is obviously the case since there are no RF chips to cause the problem) and there is no suggestion of the claimed solution.

Rejection under 35 U.S.C. 103(a) – claims 10-12, 19 and 20

In the context of the main invention, claims 10-12, 19 and 20 are secondary. These claims are directed to a specific means for achieving electrical isolation between

RF and digital chips, i.e. the use of a Faraday cage. Claims 10-12 claim a Faraday cage isolating a solder bump interconnection. Claims 19 and 20 claim a Faraday cage that is made with solder bumps.

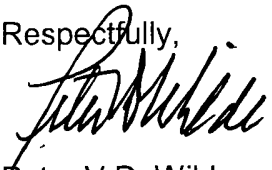
The Akram et al. patent says nothing about a Faraday cage. That is only logical since the IC chips in the Akram et al. patent are digital IC chips and a Faraday cage is relevant to RF IC chips. The rejection relies on the Vendramin patent to complete the claimed combinations. The Vendramin patent describes the use of solder balls in connection with EMI (electrical) shielding of HF (RF) signals. However, there is no basis for combining the teachings of Akram et al. with those of Vendramin in the manner of the rejection. Since there are no HF (RF) devices in the Akram et al. arrangement, there is no point whatever in resorting to the Vendramin teaching.

CONCLUSION

Accordingly it is believed that claims 1, 10-12. and 19-21 distinguish from the cited references and define patentable subject matter. Allowance of these claims is requested.

In the event that the Examiner concludes that a telephone call would advance the prosecution of this application, the Examiner is invited and encouraged to call the undersigned attorney at Area Code 757-258-9018.

Respectfully,



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